REMARKS

Claims 1 and 3-14 have been withdrawn from consideration. No new claims have been added.

Claim 2 (the remaining claim) has been rejected under 35 U.S.C. §102(b) as being anticipated by ***Ohsawa et al.*** (U.S. Patent No. 6,020,626). The Examiner asserts that ***Ohsawa*** discloses a wiring pattern (**66**) on a base metal (**72**) through an insulating film (**67**), the layer of wiring is formed by electroplating (column 2, lines 21-22); selective etching the base (column 2, lines 39-41).

Claim 2 of the application recites "forming at least one layer wiring on a base made of a metal through an insulating film. . . .". There is a distinction on the placement of the insulating film and the timing of the step of placing the insulating film between ***Ohsawa*** and the application. The fundamental difference between the present application and ***Ohsawa*** is that in ***Ohsawa***, a wiring circuit is formed on a metal base directly by electrolytic plating. In the present invention, an insulating film is formed on a metal base first except for the electric connection portions, a metallized layer is formed on that insulating film and a wiring circuit is formed thereon by elecrolytic plating.

The effects derived from the above difference are as follows:

In the ***Ohsawa*** reference, the base metal and the circuit are short-circuited electrically and the corresponding base metal portion must to be removed, however, in the present invention, the base metal and the circuit are insulated through an insulating film, so that there is no need of removing the base metal.

From the above in the present invention, the following applications which are not available in the reference can be obtained, that is:

(1) three dimensional connecting terminals are formed by removing the base metal while retaining a terminal portion,

(2) by retaining the base metal corresponding circuit wiring, such retained portions of the base metal are used as an electric source plane layer and a ground layer,

(3) by retaining the base metal under the circuit wiring while removing an LSI chip accommodating portion of the base metal as a ball grid alley (BGA) substrate, it functions as a heat spreader thus attaching an extra heat spreader layer is not necessary,

(4) by forming metal bumps, primary terminals (connected to pads of LSI chip) for mounting flip chips are formed, therefore there is no need to apply any wafer bump, and

(5) by the present invention, secondary terminals of a chip size package can be formed. For reference, normally, solder balls are mounted after packaging.

In view of the amendment to the title and the Abstract, and the above remarks, it is believed that the application is now in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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